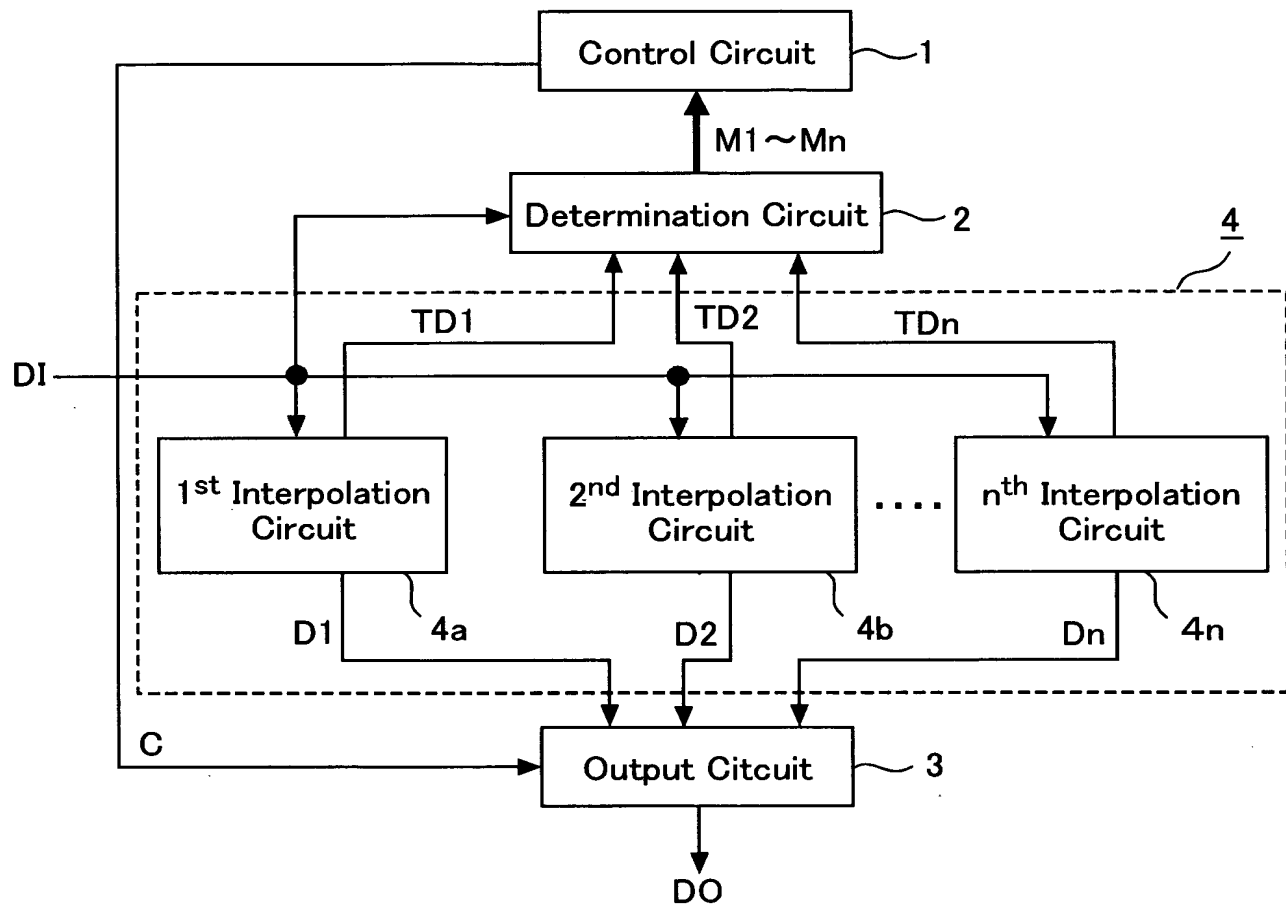


FIG. 1



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FIG.2

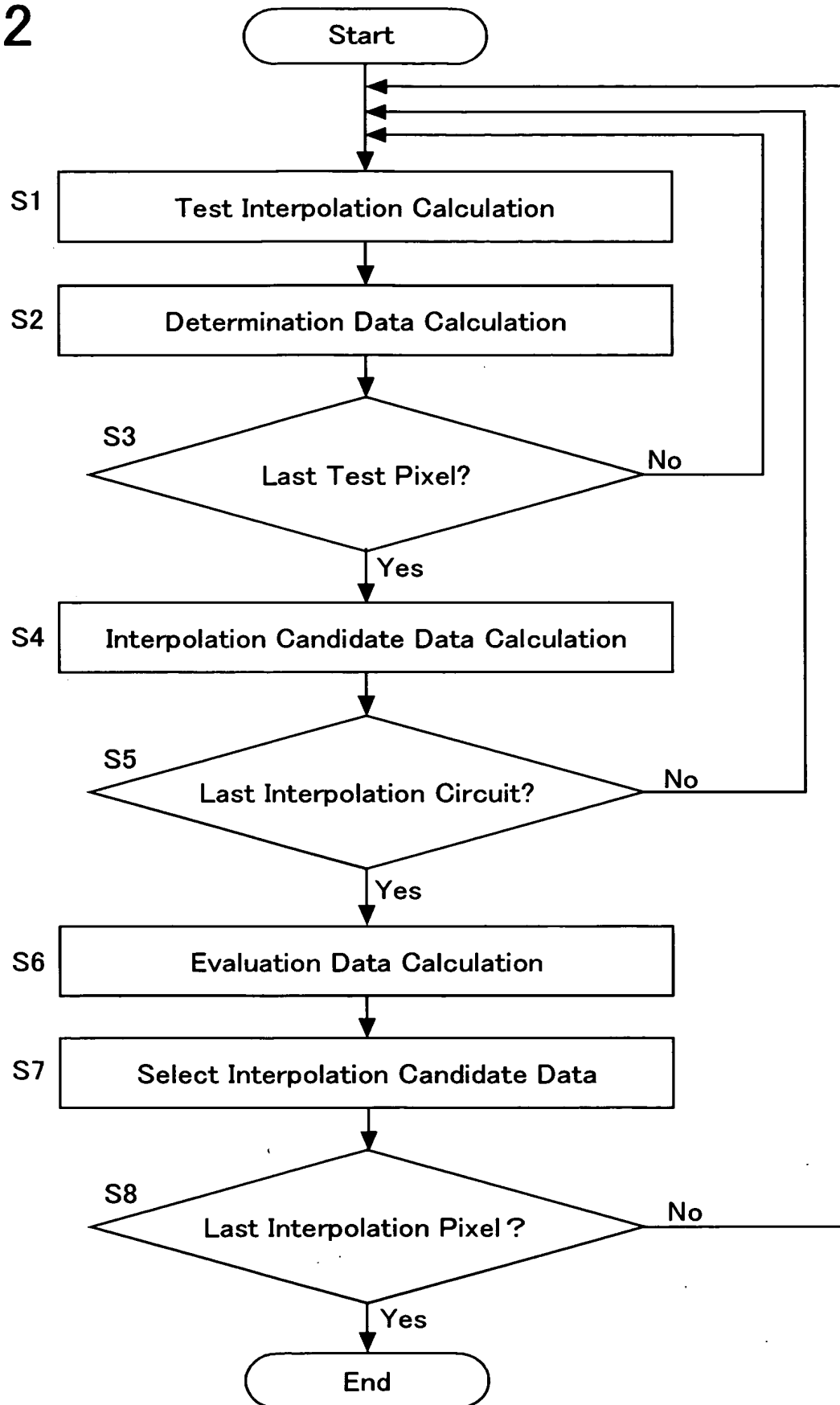
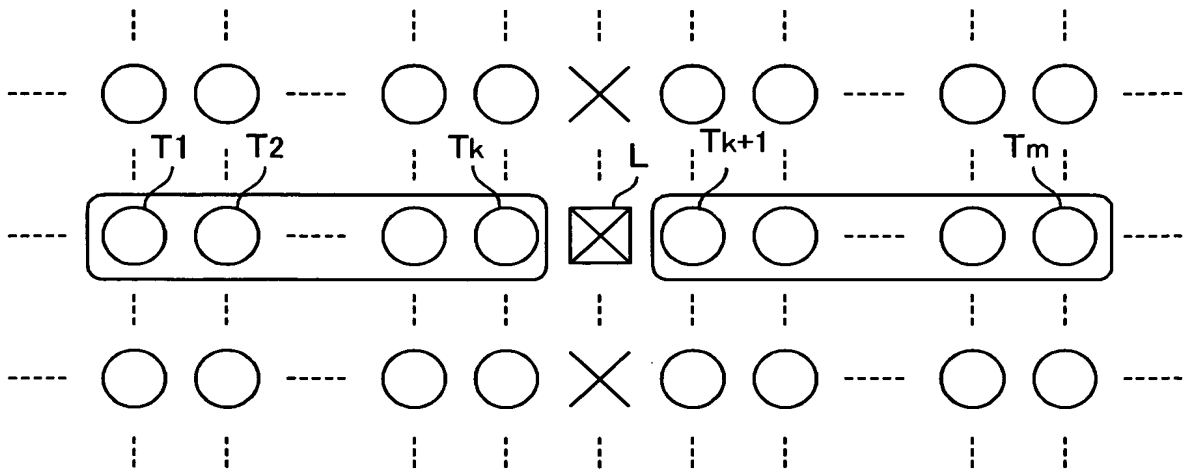
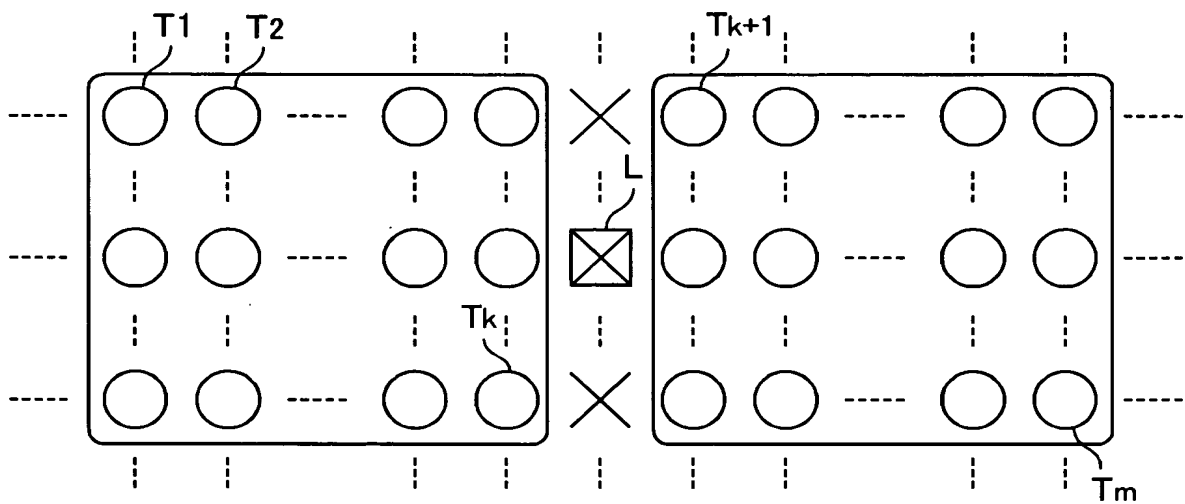


FIG.3



(a)



(b)

FIG.4

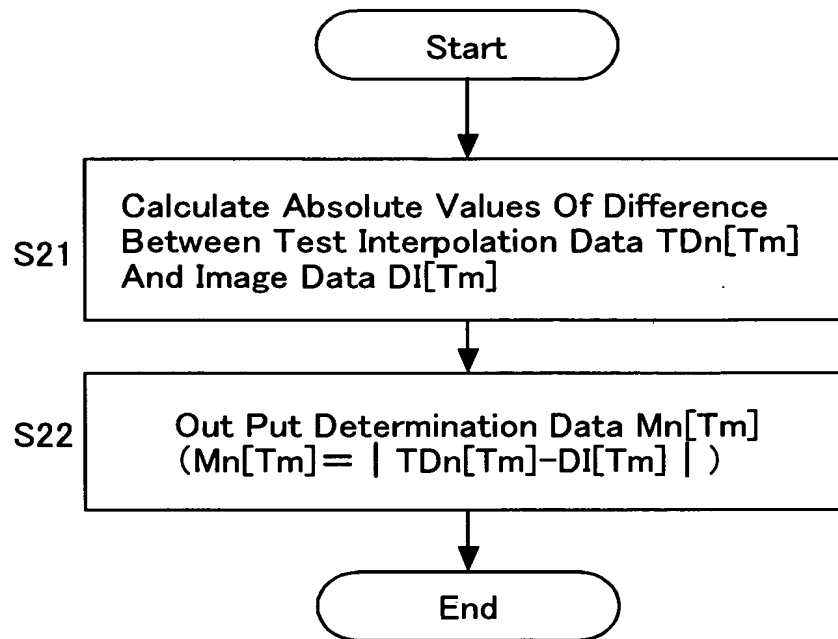


FIG.5

	T ₁	T ₂	T _m
1 st Interpolation Circuit	M1[T ₁]	M1[T ₂]	M1[T _m]
2 nd Interpolation Circuit	M2[T ₁]	M2[T ₂]	M2[T _m]
⋮	⋮	⋮		⋮
n th Interpolation Circuit	Mn[T ₁]	Mn[T ₂]	Mn[T _m]

FIG.6

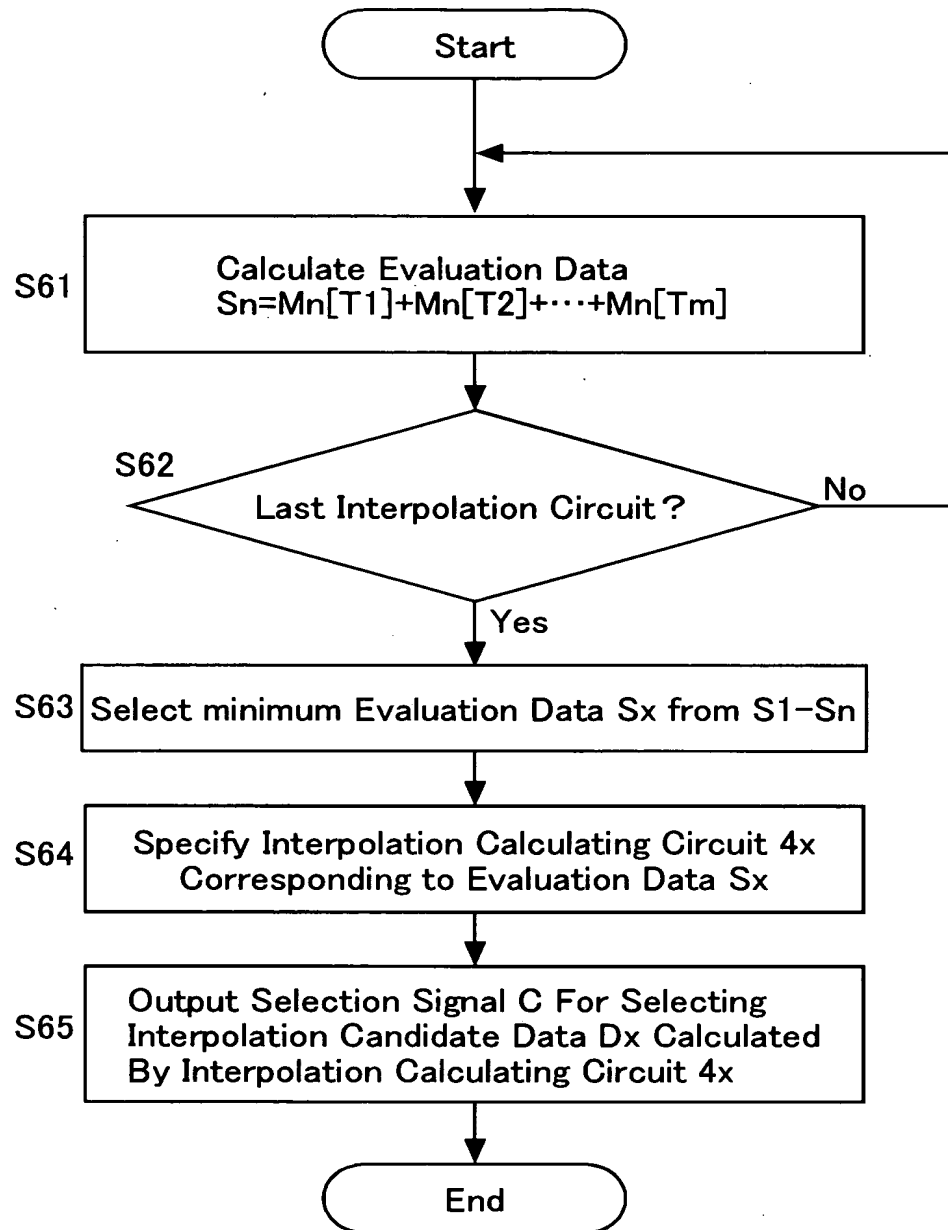


FIG.7

1 st Interpolation Circuit	S1
2 nd Interpolation Circuit	S2
⋮	⋮
n th Interpolation Circuit	Sn

FIG.8

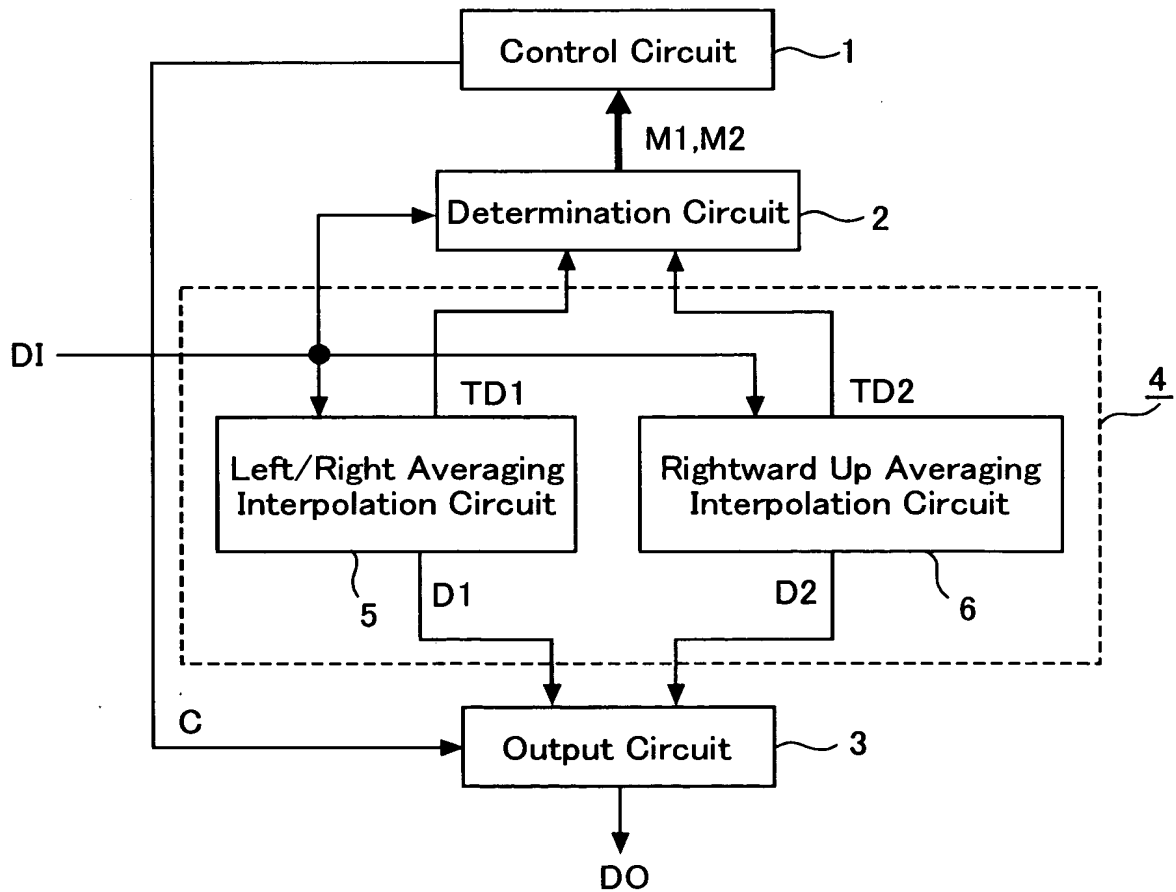


FIG.9

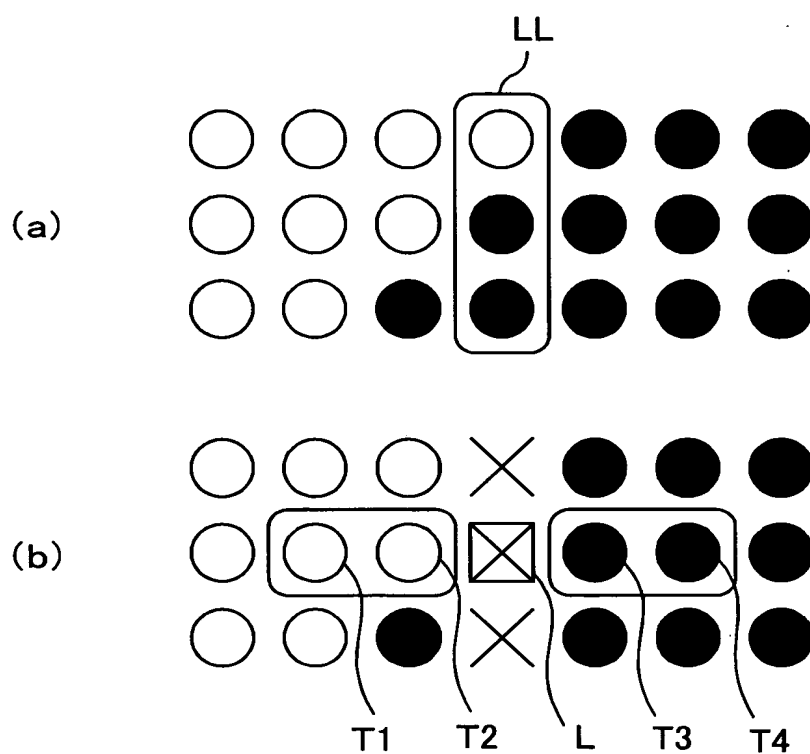


FIG.10

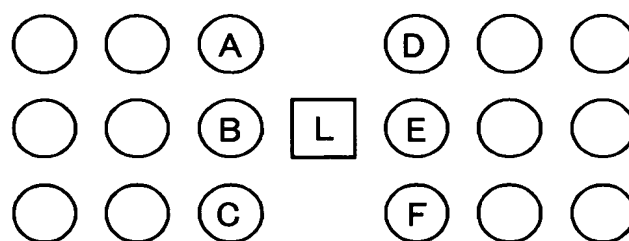


FIG.11

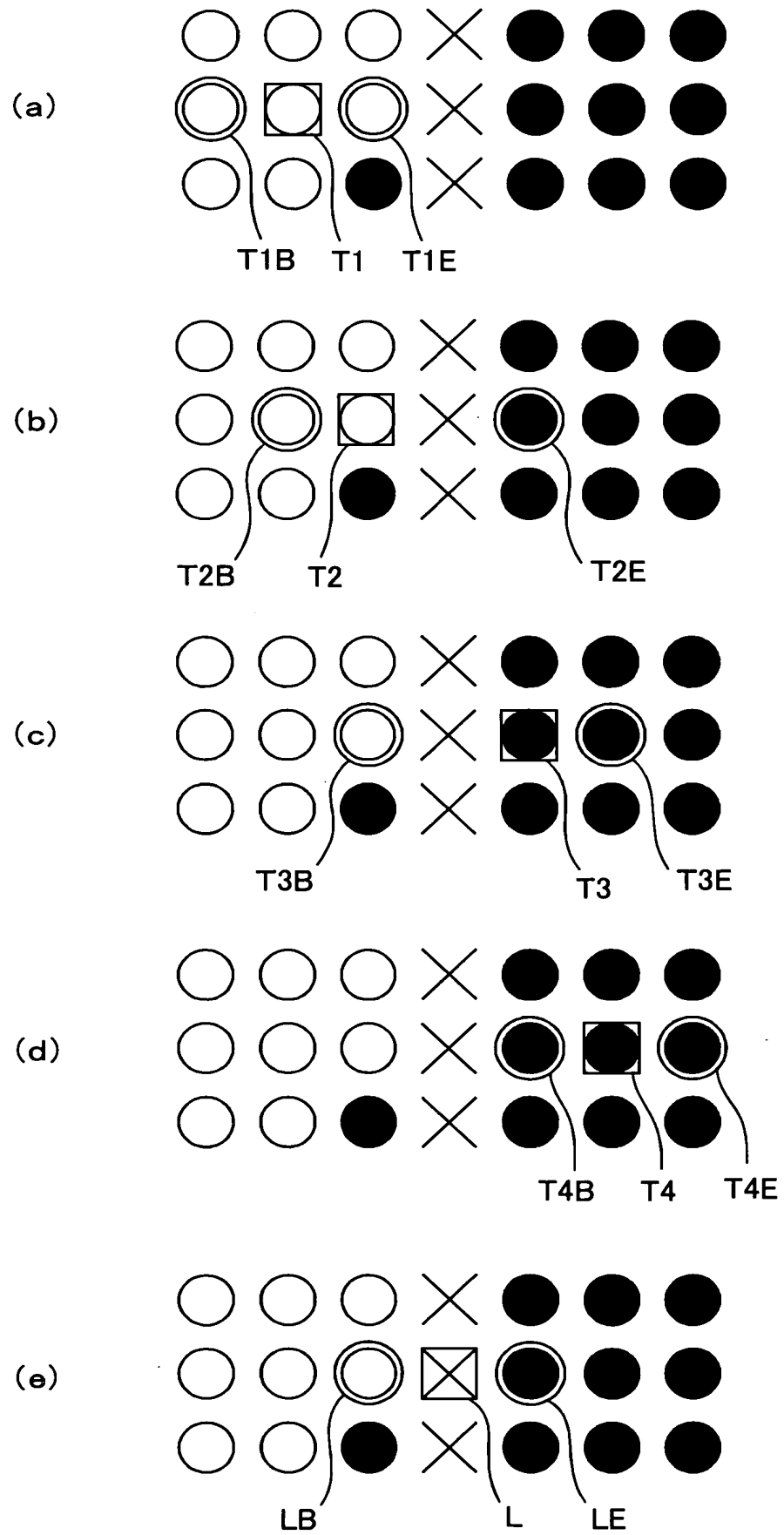


FIG. 12

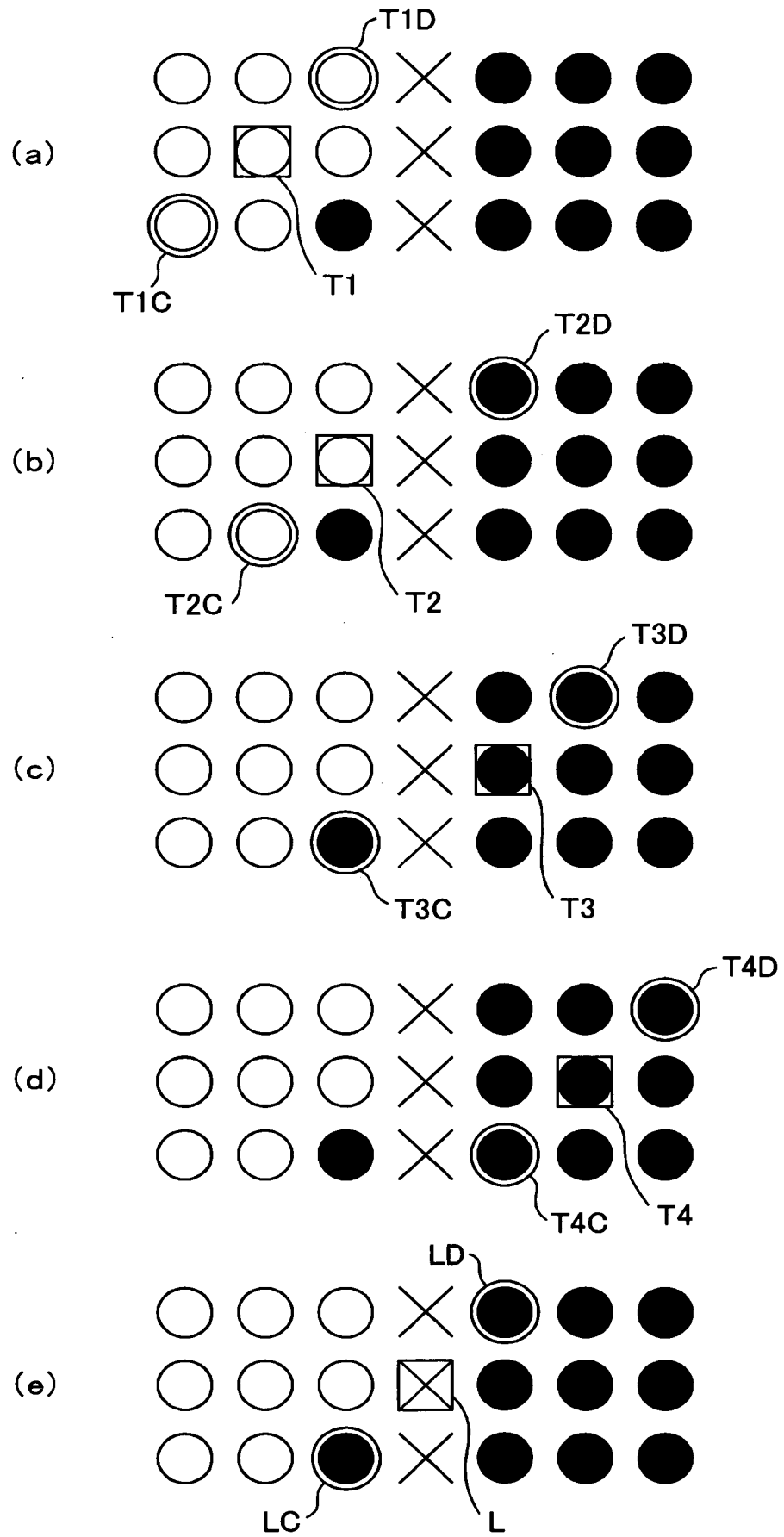


FIG.13

	T1	T2	T3	T4
M1	0	127.5	127.5	0
M2	0	127.5	0	0

FIG.14

S1	255
S2	127.5

FIG.15

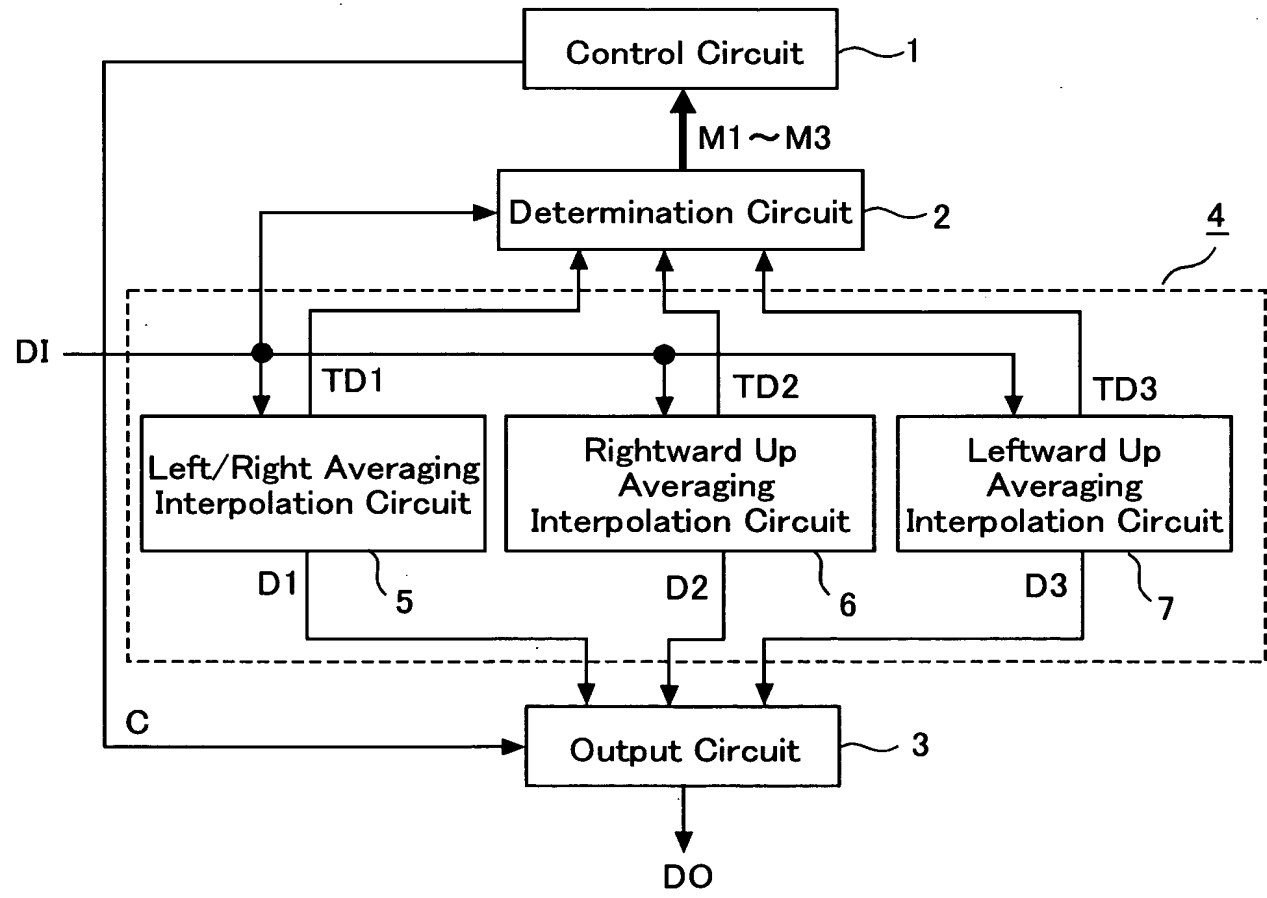


FIG. 16

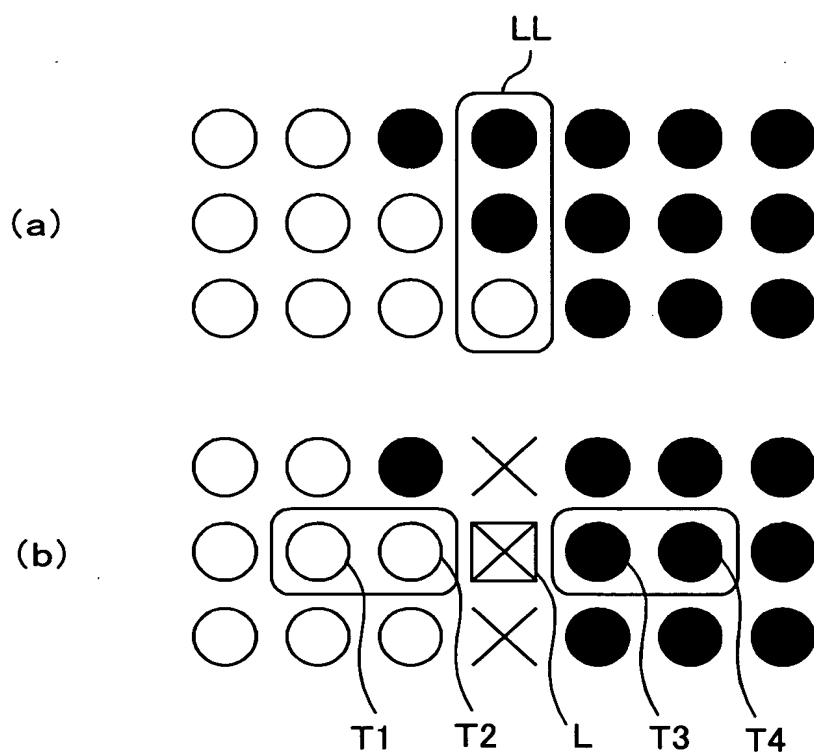


FIG.17

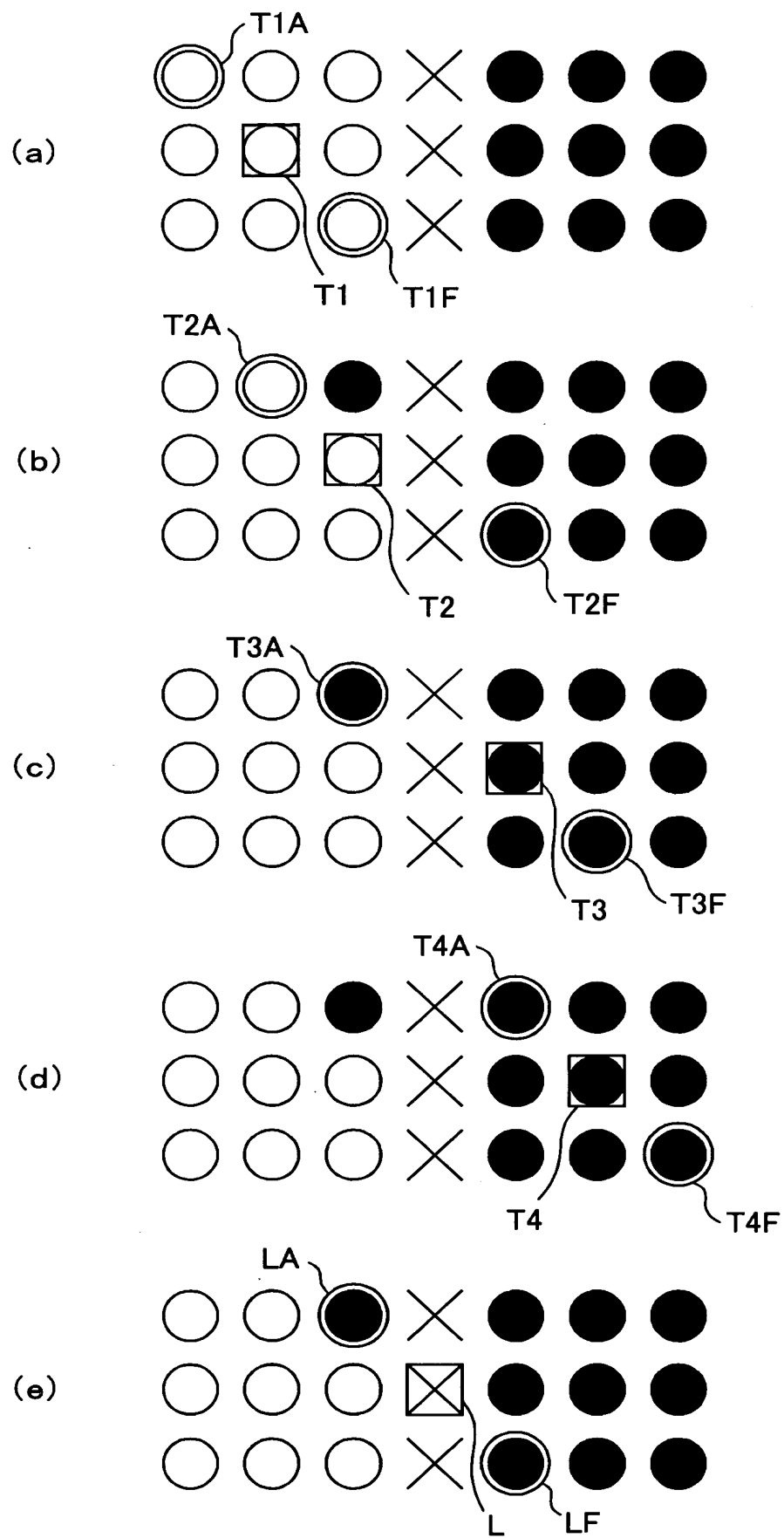


FIG.18

	T1	T2	T3	T4
M1	0	127.5	127.5	0
M2	127.5	127.5	127.5	0
M3	0	127.5	0	0

FIG.19

S1	0
S2	-2

FIG.20

	T1	T2	T3	T4
M1	-1	1	1	-1
M2	-1	1	-1	-1

FIG.21

S1	255
S2	382.5
S3	127.5

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